BROADCOM Release Notes: GCA Release: CtrlFw_Ph_24.0 - 24.00.00.00 Firmware

ReleaseOrder ID:	*DCSG01272702*
Headline:	*GCA Release: CtrlFw_Ph_24.0 - 24.00.00.00 Firmware*
Release Version:	*24.00.00.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_24.0*
UCM Stream:	*CtrlFw_Ph_24.0_Rel*
Release Type:	*GCA*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_24.0-2022-07-25-24.00.00.00_REL_1658732486@\SAS35*
Release Date:	*2022-07-25 07:00:12.000000*
Date Generated:	*Aug 01, 2022*

Release History

ReleaseOrder ID:	*DCSG01261430* Open In CQWeb
Headline:	*ReleaseCandidate Release: CtrlFw_Ph_24.0 - 23.250.12.00 Firmware*
Release Version:	*23.250.12.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_24.0*
UCM Stream:	*CtrlFw_Ph_24.0_Rel*
Release Type:	*ReleaseCandidate*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_24.0-2022-07-08-23.250.12.00_REL_1657271476@\SAS35*
Release Date:	*2022-07-08 09:10:20.000000*
Date Generated:	*Aug 01, 2022*

Defects Fixed (1):

ID: DCSG01258013
Headline: Update NVDATA Major version
Description Of Change: Update NVDATA Major version
Issue Description: Not applicable
Steps To Reproduce: Not applicable

ReleaseOrder ID:	*DCSG01254110* Open In CQWeb
Headline:	*Beta Release: CtrlFw_Ph_24.0 - 23.250.11.00 Firmware*
Release Version:	*23.250.11.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_24.0*
UCM Stream:	*CtrlFw_Ph_24.0_Rel*
Release Type:	*Beta*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_24.0-2022-06-29-23.250.11.00_REL_1656492208@\SAS35*
Release Date:	*2022-06-29 08:42:39.000000*
Date Generated:	*Aug 01, 2022*

Defects Fixed (1):

ID: DCSG01252414
Headline: Revert SATA Init timeout changes
Description Of Change: Changed SATA Init timeout from 6s to 3s.
Issue Description: Recently due to a particular drive taking long time to complete SATA Init, the SATA Init timeout was increased to 6s. This is to revert the changes.
Steps To Reproduce: Not applicable.

ReleaseOrder ID:	*DCSG01244428* Open In CQWeb
Headline:	*Beta Release: CtrlFw_Ph_24.0 - 23.250.10.00 Firmware*
Release Version:	*23.250.10.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_24.0*
UCM Stream:	*CtrlFw_Ph_24.0_Rel*
Release Type:	*Beta*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_24.0-2022-06-14-23.250.10.00_REL_1655273822@\SAS35*
Release Date:	*2022-06-15 06:15:52.000000*
Date Generated:	*Aug 01, 2022*

Defects Fixed (3):

ID: DCSG01227332
Headline: Data Corruption observed when diagnostic register dump is performed while running IO to the drives.
Description Of Change: Removed RxEEDP Buffer dump from the diagnostic register dump.

Issue Description: As part of diagnostic register dump RxEEDP buffer is also read, however if the link is up and IOs are in progress then reading this buffer can corrupt the buffer leading to wrong data getting DMA to host for a read IO.
Steps To Reproduce: Perform diagnostic register dump periodically while running IOs to the SAS/SATA drives connected to the controller.

ID: DCSG01234654
Headline: IT controller firmware sending MCTP version numbers in reverse order
Description Of Change: MCTP version number should follow BE (Big Endian)format. But controller firmware sending in LE(Little Endian) format. So changed the MCTP version number order.
Issue Description: MCTP version number should follow BE(Big Endian) format. But controller firmware sending in LE(Little Endian) format
Steps To Reproduce: Run BMC Emulator discovery and check bmcPCIeEndptUtil output for MCTP versions.

ID: DCSG01231494 (Port Of Defect DCSG01161733)
Headline: Change spinup mode while SATA link reset is occurring
Description Of Change: When a task management causes a SATA link reset to occur, firmware temporarily changes the spinup mode type before resetting the link. The new spinup mode bypasses the hold state and completes the reset sequence without delaying or requiring a new spinup request. Once a link signal is received, the original spinup mode is restored, allowing for normal spinup operation when a drive is replaced.
Issue Description: Configuration pages allow end users to specify both the maximum number of devices undergoing spinup and the minimum time between spinup notifications. End users may adjust these settings as desired to maximize power supply use within safe operating parameters. If firmware has recently sent a spinup request to the maximum number of devices specified, the specified delay period must be adhered to before a new spinup request may be sent.

When a SATA target reset occurs, the link to the SATA drive drops. A new spinup request is required for link up to occur. If the maximum allowed number of drives are currently undergoing spinup and the remaining spinup delay time for these drives exceeds the target reset timeout, the target reset may time out before link up can occur.

Upon receiving a failed target reset status, the driver will issue a controller reset. This is currently interpreted as a F000 fault.
Steps To Reproduce: Connect legacy (pre SPL-2) SAS drives, which require periodic spinup requests, consuming the maximum spinup device spinup requests. Set the spinup delay to 12 seconds and issue target reset task managment messages to a direct attached SATA drive.

ReleaseOrder ID: ***DCSG01233562*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_24.0 - 23.250.09.00 Firmware***
Release Version: ***23.250.09.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-06-03-23.250.09.00_REL_1654263632@\SAS35***
Release Date: ***2022-06-03 13:38:03.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (2):

ID: DCSG01194600
Headline: [SATA] SATA Initialization fails on certain large capacity SATA drives
Description Of Change: Increased the SATA Initialization timeout to 6 seconds from 3 seconds.
Issue Description: Certain large capacity SATA SSD take long time to respond for Read Log Ext commands sent during SATA Initialization. That leads to SATA Initialization to time out, even after a few retries the it is not able to complete initialization so host marks the drive as failed.
Steps To Reproduce: Hot plug a specific OEM large capacity (more than 6TB) SATA SSD to the controller and observe that drive fails to get added in OS.

ID: DCSG01230479
Headline: Locate LED operation does not work for NVMe drive slot on UBM backplane
Description Of Change: UBM stack has been updated to transition correct states for command operations.
Issue Description: The locate LED operation, for NVMe drive slot on UBM backplane, would not respond to LED control commands from storcli on certain OEM UBM backplanes.
Steps To Reproduce: Issue LED control command from storcli to NVMe drive slot's Locate LED.

ReleaseOrder ID: ***DCSG01229152*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_24.0 - 23.250.08.00 Firmware***
Release Version: ***23.250.08.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-05-31-23.250.08.00_REL_1653987887@\SAS35***
Release Date: ***2022-05-31 09:03:44.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (3):

ID: DCSG01224310
Headline: Possible division or modulo by zero in enclosure management code.
Description Of Change: Added a check to see if variable is non zero before using it for modulo operation.
Issue Description: Possible modulo by zero code while converting connector lane to controller phy during enclosure management code.
Steps To Reproduce: Not applicable.

ID: DCSG01224346
Headline: Phase 24 Code analysis tool Defects related to SPDM
Description Of Change: Fixed Code analysis tool reported issues related to SPDM files
Issue Description: The code analysis tool reported Uninitialized variable issues in the latest SPDM platform code.
Steps To Reproduce: Run Code analysis tool

ID: DCSG01225064
Headline: Uninitialized pointer access in UBM Backplane management code.
Description Of Change: Added a null pointer check before accessing the variables from print statement.
Issue Description: Uninitialized Pointer variables are accessed in a print statement.
Steps To Reproduce: Not applicable.

Enhancements Implemented (1):

ID: DCSG01224363
Headline: Update SB Lib to latest
Description Of Change: Updated firmware component baseline to use latest SBLI Version : 0x02060000.

ReleaseOrder ID: ***DCSG01222500*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_24.0 - 23.250.07.00 Firmware***

Release Version: ***23.250.07.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-05-23-23.250.07.00_REL_1653304753@\SAS35***
Release Date: ***2022-05-23 11:18:21.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (2):

ID: DCSG01207008
Headline: HBA discovery failed with Phase 24 Storelib and StorelibTest
Description Of Change: Fixed the error check in I2C read callback, so the I2C read Toolbox command is failed appropriately on receiving address NAK.
Issue Description: As part of HBA discovery, StorelibTest sends Toolbox command to read PSOC version using I2C. In some 9500-8e controllers there is no PSOC present, so I2C read is failed with NAK. Due to a bug in firmware this error was ignored and it kept waiting for data resulting in Toolbox command timeout.
Steps To Reproduce: Boot to OS with 9500-8e card connected, use Phase 24 Storelib and StorelibTest and run HBA discovery. HBA discovery failed due to timeout.

ID: DCSG01222353 (Port Of Defect DCSG01220829)
Headline: IOC Page 7 does not report the updated "SASNotifyPrimitiveMasks"
Description Of Change: Fixed the IOC config page read callback, so the IOC config Page 7 SASNotifyPrimitiveMasks field is updated in the host read buffer.
Issue Description: As part of a manual testing to set and unset all of the event masks. Host sent command to change the MPI event masks in IOC config page 7and then read back the modified page. But due to one bug in firmware SASNotifyPrimitiveMasks field was not populated in host read buffer hence remained unchanged during config page read data.
Steps To Reproduce: Send Event Notification MPI with all the events to 0xFF
Read IOC Page 7 using ScrutinyCLI
See SASNotifyPrimitiveMasks set to 0x00 instead of 0xFF

ReleaseOrder ID: ***DCSG01219365*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_24.0 - 23.250.06.00 Firmware***
Release Version: ***23.250.06.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-05-18-23.250.06.00_REL_1652868934@\SAS35***
Release Date: ***2022-05-18 10:14:19.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (6):

ID: DCSG00428841
Headline: SPILIB2: Fix offsets in SPI2_LIB_DEVICE_PARAMS
Description Of Change: Fixed offsets in SPI2 structure comments
Issue Description: During code inspection it was noted some comments were wrong
Steps To Reproduce: Review SPI2 header files

ID: DCSG00814654
Headline: SPILIB2 : Watchdog reset due to ARM Exception while flash under stress
Description Of Change: Set the suspend bits correctly for commands with no address or data phases (i.e. resume command)
Issue Description: The ARM freezes on the second resume due to the suspend enable bits getting cleared by the first resume
Steps To Reproduce: Force two or more suspend/resume cycles during a single erase or write to flash when suspend is enabled.

ID: DCSG00914933
Headline: SPILIB2: (Margay Only) ARM Exception while flash under stress upon closing telnet
Description Of Change: Ensured suspend bits were set for all manual commands
Issue Description: Resume command cleared the suspend enable bits in the manual register
Steps To Reproduce: (Margay only)
1. Build run from flash firmware CLI module in flash.
Download to board all regions and reset.
Make sure the board has unique IP address for telnet connection.
2. Now open 4 telnet sessions using tera term and start following macro on respective sessions.
log_entry.ttl, tftp_ful_80.ttl, tftp_ful_82.ttl, telnet_stress.ttl
3. Connect FW CLI using tera term, and run macro tffp_fdl.ttl
4. Let all macros run for 10 mins.
5. Start closing the telnet sessions one by one at some interval
While closing telnet sessions, margay experience ARM Exception, does watchdog reset.
There is not issue unless telnet sessions are closed.

ID: DCSG01049441
Headline: SPILIB2: SPI Emulation Erases the wrong section
Description Of Change: Fixed starting address calculation
Issue Description: In the SPI flash emulation archive only:
The emulation was calculating the start of the flash sector incorrectly and was erasing the wrong area
Steps To Reproduce: In a system which uses the emulation instead of real silicon, erase a sector at a non-zero offset.

ID: DCSG01182027
Headline: SPILIB2: Series 9700 Chip Select Timing registers default to zero
Description Of Change: Added code to initialize the CS1 registers which are not initialized by either hardware or SBR
Issue Description: The Chip Select Timing registers default to zero which is a value unexpected by SPI state machines
Changed the value before initialization to avoid SPI manual mode failures.
Steps To Reproduce: Load the 22_04_05 bitstream with spi bootleg and run the rmtflash NVSRAM SPI test

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ID: DCSG01215896 (Port Of Defect DCSG01200427)
Headline: [VSes] Number of slots reported incorrectly in certain OEM backplane.
Description Of Change: Add a check to see if phy is part of phys with PCIe enabled before setting Invalid bit for the additional element descriptor corresponding to the phy based on PCIe link configuration.
Issue Description: To report a single slot for the phys belonging to a PCIe link, invalid bit is set in the additional element descriptor for all phys other than the first phy of the PCIe link. In certain backplane where only some phys/slots are PCIe enabled and other phys are SAS/SATA only and since Link of all phys is initialized to 0 caused some elements to be incorrectly marked invalid.
Steps To Reproduce: Attach OEM backplane to the controller and read number of slots by checking the number of valid element descriptors in SES Page 0Ah of the VSes.

Enhancements Implemented (18):

ID: DCSG00424412
Headline: SPILIB2: Support for Additional SPI Clock Frequencies

Description Of Change: Add enumerations and supporting code for additional clock frequencies
NOTE: Requires external configuration of reference clock for some chips

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ID: DCSG00429625
Headline: SPILIB2: Support ECC for Margay
Description Of Change: Margay has special ECC Hardware in the SPI Core
This will add an option to set Read ECC Enable
NOTE! Write data must be manually calculated and interrupts externally configured

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ID: DCSG00508974
Headline: SPILIB2: Add High Level SPI Emulation Library
Description Of Change: Add emulation library

ID: DCSG00734502
Headline: SPILIB2: Add support for new Cypress parts via proprietary CFI Method
Description Of Change: Currently SPILIB2 only supports production parts which do not include the Cypress hybrid sector parts
Add CFI support for the 256MBit and 128MBit parts so that the library can distinguish between the two parts
(RDID is the same for both hybrid and uniform sector parts of these chips)

ID: DCSG00782279
Headline: SPILIB: Add support for Hybrid topology CFI parts
Description Of Change: Add product-specific erase command configuration for Hybrid CFI parts

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ID: DCSG00830450
Headline: SPILIB2: Eliminate incompatible erase commands in MultiErase mode
Description Of Change: Winbond 256MBit parts do not support the 32K erase type as 4-byte
This removes that option from the user information

ID: DCSG00831421
Headline: SPILIB2: Add support for serial mode for parts with QE=1 and dual mode support
Description Of Change: Per the coding standard, change flash size constants to a definition

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ID: DCSG00916467
Headline: SPILIB2: Add serial mode support for SPI devices with read only Quad Enable bits. Add hybrid dual mode support.
Description Of Change: Added more support for serial mode in SPI devices that have a read only QE (Quad Enable) bit
NOTE! This requires the UseFactoryDefaults bit to be set as an override as there is a requirement to clear QE in some situations
Also added new (Hybrid) Dual mode.
Since there are no dual write commands in the supported devices this will require RequireMatchedCmds to be zero.
One may also use this command with read only QE devices by setting the aforementioned WpDontCare bit.

ID: DCSG00917802
Headline: SPILIB2: Port all changes AV1 to AV2 for manual access files
Description Of Change: Ported all changes since 20.00.11.00 from Aero/AV1 to the only unique file, spi2ManualAvg.c
Also moved suspend function to a separate file as those need to be managed separately and be in a different object module
In addition there we small changes to the GHS environment so that it always matches the target configuration and links properly

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ID: DCSG00943761
Headline: SPILIB: Update build scripts for ADS
Description Of Change: Updated the build script to point to the new install directory, C:\ARM\5P06U7\bin
In order to better support other compilers, ALTERNATE_GHS_PATH should be set to the GHS installation path and ALTERNATE_ARM_PATH to the ARM installation path in the future. Otherwise the compilers must be installed in the firmware specified location.

ID: DCSG00980221
Headline: SPILIB: Add Python-Based Logic Analyzer Decoder
Description Of Change: Added a python script to support debug of large traces

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ID: DCSG01015117
Headline: SPILIB2: Add new configuration bits to the init interface for SPI Flash drive strength
Description Of Change: Added internal option to specify SPI flash drive strength

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ID: DCSG01117315
Headline: SPILIB: Update Series 9700 header file
Description Of Change: Update headers to 12/9/21 at 11:21:39 version

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ID: DCSG01118681
Headline: SPILIB2: Add support for high impedance dummy cycles in 9700 Series
Description Of Change: Add support for new high impedance dummy cycle option for 9700 Series Controllers

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ID: DCSG01131779
Headline: SPILIB2: Configure Series 9700 NVSRAM hardware to send Write Enable on first auto-write
Description Of Change: In order to ensure the NVSRAM is writable, set up the hardware to send a Write Enable command on the first write
Also add a Write Enable command to the normal init path in order that the SPILIB init might be called a second time without issues

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ID: DCSG01170965
Headline: SPILIB2: 9700 Series core needs maximum continuous count initialized earlier
Description Of Change: Initialized the maximum continuous count register to a small value so that manual mode requests might be honored.
The default was infinity.

ID: DCSG01209350
Headline: Add ApSHA changes
Description Of Change: Added below changes-

Use SHA 384
Use finalize bit instead of byte count

ID: DCSG01215946
Headline: Update SPI Lib to latest

Description Of Change: Updated firmware component baseline to use latest SPI lib version (20.00.32.00). Fixed some build issues.

ReleaseOrder ID: ***DCSG01207721*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_24.0 - 23.250.05.00 Firmware***
Release Version: ***23.250.05.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-05-06-23.250.05.00_REL_1651827742@\SAS35***
Release Date: ***2022-05-06 08:58:21.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (2):

ID: DCSG01194126
Headline: Disable SATA protocol when in optical mode
Description Of Change: Disable SATA (set SASOnly in the phy registers) for the phys that have optical cable connected
Issue Description: While running link reset test with controller connected to an Expander with certain optical cable, it is observed that some phys don't negotiate at correct speed or fail to link up.
Steps To Reproduce: Run link reset test on phys connected to an expander with optical cable and check the link negotiation failure.

ID: DCSG01196230
Headline: Hardware Workaround:Link between Controller and expander not always recovering after link reset
Description Of Change: Updated 95xx controller Combo Serdes Wrapper firmware to latest that includes link stability fixes for optical cables.
Issue Description: When the link between controller and expander connected using an optical cable is reset, sometimes the phys don't link up at expected speed or not link up at all.
Steps To Reproduce: Attach an expander to controller using specific optical cables. Reset controller a few times and observe that either the link speed of phys in not as expected or they do not link up.

Enhancements Implemented (4):

ID: DCSG01142850
Headline: [Code Coverage] Include Task Management tests for VSES
Description Of Change: Included below Task Management commands for Virtual SES

1- Abort Task
2- Abort Task Set
3- Target Reset
4- Lun Reset
5- Clear Task Set
6- Query Task
7- Query Task Set

ID: DCSG01142851
Headline: [Code Coverage] Include Read Buffer commands in VSES BST
Description Of Change: Included below Read buffer commands for Virtual SES

1- UBM Receptacle ID List - Buffer ID F0h
2- UBM FRU Data - Buffer ID F1h
3- UBM FRU Valid PRIDs - Buffer ID F2h
4- UBM Controller Data - Buffer ID F3h
5- UBM Controller Command Data - Buffer ID F4h

ID: DCSG01154617
Headline: [Code Coverage] Include Write Buffer commands in VSES BST
Description Of Change: In order to execute Write Buffer commands for Virtual SES, I have added below commands in BST

1- Enter Programmable Update Mode - Buffer ID F5h
2- Exit Programmable Update Mode - Buffer ID F6h
3- Programmable Mode Data Transfer - Buffer ID F7h

ID: DCSG01176573
Headline: BST: Update UART ports for BST Testhosts in scripts.
Description Of Change:
BST scripts were updated as per latest hardware and UART port config.

ReleaseOrder ID: ***DCSG01199095*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_24.0 - 23.250.04.00 Firmware***
Release Version: ***23.250.04.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_24.0***
UCM Stream: ***CtrlFw_Ph_24.0_Rel***
Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_24.0-2022-04-28-23.250.04.00_REL_1651142728@\SAS35***
Release Date: ***2022-04-28 10:43:18.000000***
Date Generated: ***Aug 01, 2022***

Defects Fixed (2):

ID: DCSG01194141
Headline: Self test aborts when Open Zone command issued on a Security locked drive
Description Of Change: Moved background self-test activation pending flag clearing logic from SATA initialization to end of task management.
Issue Description: When SATA drive is in security locked state if controller receives any command which is not supported in locked state then firmware fails that command and triggers SATA initialization to detect the actual state of security lock for next command. During SATA initialization background self-test flag cleared hence it was reported as completed during SATA SCSI Request Sense.
Steps To Reproduce: Put the drive in security locked state, start back ground self-test, check the self-test progress, send read or write command, check self test status. Found that the self-test completed.

ID: DCSG01196465 (Port Of Defect DCSG01193134)
Headline: [NVMe] Some NVMe drives do not link up on certain OEM backplanes.
Description Of Change: Revert changes where Refclk is not enabled for SGPIO backplane type.
Issue Description: The backplane type GPIO on an OEM backplane that supports NVMe drives was set to SGPIO instead of I2C. Due to a recent defect fix on connector modules where the backplane type was set to SGPIO the RefClk was not enabled. This leads to NVMe drives not linking up on those phys.
Steps To Reproduce: Attach a few NVMe drives to the connector using certain OEM backplane. Observe that some of the NVMe drives are not discovered.

ReleaseOrder ID: ***DCSG01194929*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_24.0 - 23.250.03.00 Firmware***
Release Version: ***23.250.03.00***

UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_24.0*
UCM Stream: *CtrlFw_Ph_24.0_Rel*
Release Type: *Pre-Alpha*
State: *Released*
Release Baseline: *CtrlFw_Ph_24.0-2022-04-25-23.250.03.00_REL_1650886617@\SAS35*
Release Date: *2022-04-25 11:36:01.000000*
Date Generated: *Aug 01, 2022*

Defects Fixed (3):

ID: DCSG01178348
Headline: [Aero/Ventura] Add check for Sense Data size
Description Of Change: FW fix for the FW Memory crash issue due to Sense data size (SAS drive returned 14 byte, FW expectation is min 18 byte).

FW fix - Added a Sense Data Length check before accessing Sense data buffer in FW.
Issue Description: Some drives have sense data length less than the spec mandated minimum size. This causes memory access fault on controller FW.
This activity will add a check for sense data size.
Steps To Reproduce: 1- Use a drive that has sense data length of less than 18 bytes.

ID: DCSG01183332
Headline: LBA information missing from sense data with Medium Error Sense Key for SATA drives.
Description Of Change: Populate LBA information for all ASC/ASCQ for Read error causing Medium error. And set valid LBA in SenseData for all ASC/ASCQ for Read Error causing Medium error.
Issue Description: LBA information not updated if the drive reports sense key as medium error and ASC/ASCQ 1114(SCSI_ASC_READ_ERROR_LBA_MARKED_BAD_BY_APPLICATION_CLIENT)
Steps To Reproduce: 1. Inject medium error on an LBA of a SATA drive that supports sense data available.
2. Issue SCSI verify command
Some drives report sense Key Medium error and ASC/ASCQ 1114(SCSI_ASC_READ_ERROR_LBA_MARKED_BAD_BY_APPLICATION_CLIENT)

ID: DCSG01185588
Headline: Aero: Incorrect topology phys memory allocation
Description Of Change: As part of phys memory allocation in FW, FW calculates the multiplier by adding all the supported phys by the controller. During multiplier calculation in FW there was one hardcoded value (2), put for the max VSES devices.
Replacing this hardcoded value (2) with a runtime calculation of max no. VSES devices supported by the controller.
Issue Description: As part of phys memory allocation in FW, FW calculates the multiplier by adding all the supported phys by the controller. During multiplier calculation in FW there was one hardcoded value (2), put for the max VSES devices.
Steps To Reproduce: Can't reproduce

ReleaseOrder ID: *DCSG01183534* Open In CQWeb
Headline: *Pre-Alpha Release: CtrlFw_Ph_24.0 - 23.250.02.00 Firmware*
Release Version: *23.250.02.00*
UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_24.0*
UCM Stream: *CtrlFw_Ph_24.0_Rel*
Release Type: *Pre-Alpha*
State: *Released*
Release Baseline: *CtrlFw_Ph_24.0-2022-04-08-23.250.02.00_REL_1649418285@\SAS35*
Release Date: *2022-04-08 11:44:00.000000*
Date Generated: *Aug 01, 2022*

Enhancements Implemented (1):

ID: DCSG01154887
Headline: Aero FW-Download: when writing bootloader to the main region, write the signature bytes last
Description Of Change:
When copying bootloader to main region, if power was cut-off, the flash image would have valid image signatures but incomplete content.
This activity enables hardware to detect such partial image data as an invalid image,

When copying bootloader to main region, non-signature bytes are written first.
Once done, the signature bytes are written in the very end.
As a result, if power is removed during copy process, the partial image will not have valid signatures and the hardware will look elsewhere for a valid FW image.

ReleaseOrder ID: *DCSG01179884* Open In CQWeb
Headline: *Pre-Alpha Release: CtrlFw_Ph_24.0 - 23.250.01.00 Firmware*
Release Version: *23.250.01.00*
UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_24.0*
UCM Stream: *CtrlFw_Ph_24.0_Rel*
Release Type: *Pre-Alpha*
State: *Released*
Release Baseline: *CtrlFw_Ph_24.0-2022-04-05-23.250.01.00_REL_1649149266@\SAS35*
Release Date: *2022-04-05 09:00:13.000000*
Date Generated: *Aug 01, 2022*

Enhancements Implemented (2):

ID: DCSG01132478
Headline: Aero - SecureBoot: Added debug messages to the ring-buffer when the FW download operation fails
Description Of Change: Debug messages are added to the FW Ring-buffer logs when the FW-Download operation fails (e.g. due to invalid image signature etc.)
There is no functional change to the code.

ID: DCSG01137935
Headline: [SNTL] Update SCSI Format Translation for NVMe devices
Description Of Change: Added support for immediate bit in the parameter data of SCSI Format command.
Added checking for protection information, since Aero does not support protection information if fields are non zero the command is failed.
Command is failed if both FMTDATA and CMPLIST are set.
